What is claimed is:

1. A non-volatile memory device comprising:

a lower oxide layer, a charge trapping layer, an upper oxide layer, and a control gate sequentially stacked on a substrate; and

a source region and a drain junction region formed at opposite sides of the stacked lower oxide layer, charge trapping layer, upper oxide layer and control gate, wherein portions of the charge trapping layer adjacent to the source junction region and the drain junction region are thicker than remaining portions of the charge trapping layer.

2. The non-volatile memory device of claim 1, wherein the charge trapping layer includes at least two portions thereof having the shape of at least two spacers facing each other on the lower oxide layer, and the upper oxide layer and the control gate are self-aligned between the at least two spacers.

3. The non-volatile memory device of claim 2, wherein upper surfaces of the charge trapping layer, the upper oxide layer, and the control gate are level with one another.

4. The non-volatile memory device of claim 1, further comprising an ion implantation layer formed in the substrate below the lower oxide layer, the ion implantation layer for controlling a threshold voltage.

5. The non-volatile memory device of claim 1, wherein the charge trapping layer is one of a silicon nitride layer, a silicon oxy nitride layer, a layer including polysilicon dots, and a layer including nitride dots.

6. A non-volatile memory device comprising:

an ion implantation layer for controlling a threshold voltage formed in a substrate;

a lower oxide layer formed on the ion implantation layer;

a charge trapping layer formed on the lower oxide layer and having two portions thereof shaped like two spacers facing each other, the two spacers each having an inner portion shorter than an outer portion;

an upper oxide layer formed on the charge trapping layer and the lower oxide layer;

a control gate that is self-aligned on the upper oxide layer and includes a flat upper surface; and

a source junction region and a drain junction region formed in the substrate at opposite sides of the ion implantation layer.

7. The non-volatile memory device of claim 6, wherein the upper surfaces of the charge trapping layer, the upper oxide layer, and the control gate are level with one another.

8. The non-volatile memory device of claim 6, wherein the charge trapping layer is one of a silicon nitride layer, a silicon oxy nitride layer, a layer including polysilicon dots, and a layer including nitride dots.

9. The non-volatile memory device of claim 6, wherein a central portion of the control gate is etched to expose a portion of the substrate, and a common source and drain junction region is formed in the exposed portion of the substrate.

10. A method of fabricating a non-volatile memory device, comprising:

forming a lower oxide layer on a substrate;

forming a sacrificial layer on the lower oxide layer and patterning the sacrificial layer to form an opening;

forming a charge trapping layershaped like at least two spacers along an inner wall of the opening:

forming an upper oxide layer covering the sacrificial layer and the charge trapping layer, the upper oxide layer fills a portion of the opening;

forming a polysilicon layer on the upper oxide layer for filling a remaining portion of the opening;

planarizing an upper surface of the polysilicon layer until the sacrificial layer is exposed to form a self-aligned control gate in the opening;

removing the sacrificial layer and the lower oxide layer formed below the sacrificial layer; and

forming a source junction region and a drain junction region in the substrate at opposite sides of the control gate.

11. The method of claim 10, wherein the sacrificial layer is formed of a material capable of being selectively etched with respect to the charge trapping layer.

12. The method of claim 10, wherein the sacrificial layer is an oxide layer.

13. The method of claim 10, wherein the charge trapping layer is one of a silicon nitride layer, a silicon oxy nitride layer, a layer including polysilicon dots, and a layer including nitride dots.

14. The method of claim 10, further comprising performing ion implantation into the opening in the substrate for controlling a threshold voltage.

15. The method of claim 10, wherein the step of forming the charge trapping layer includes:

depositing a layer in the opening, the layer filling only a portion of the opening; and

forming spacers along an inner wall of the opening by etching back the layer until an upper surface of the sacrificial layer is exposed.

16. The method of claim 15, further comprising etching back the spacers so that a height of each spacer is less than a height of the inner wall of the opening.

17. The method of claim 10, wthe step of forming the charge trapping layer includes:

forming a layer in the opening, the layer filing only a portion of the opening; and

forming spacers along an inner wall of the opening by slope etching the layer until an upper surface of the sacrificial layer is exposed.

18. The method of claim 17, further comprising etching back the spacers so that a height of each spacer is shorter than a height of the inner wall of the opening.

19. The method of claim 10, wherein the step of planarizing is performed using chemical mechanical polishing.

20. The method of claim 10, wherein the step of planarizing is performed until the charge trapping layer is exposed.

21. The method of claim 10, further comprising performing silicidation on the control gate.

22. The method of claim 10, further comprising:

exposing the substrate by etching a central portion of the control gate; and

forming a common source and drain junction in an exposed portion of the substrate.